IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Li	Attorney Docket:	2004 P 50201 US
Filed:	Herewith	Examiner:	TBD
Serial No.:	TBD	Art Unit:	TBD

For: Transistor with Shallow Germanium Implantation Region in Channel

Mail Stop: Patent Application
Commissioner for Patents
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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a & 08b that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Respectfully submitted,

March 22, 2004
Date

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PTO/SB/08a (08-03)
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(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	TBD
Filing Date	HEREWITH
First Named Inventor	Li
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	2004 P 50201 US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-6,621,131 B2	09-16-2003	Murthy, *et al.*	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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Sheet 2 of 2

Complete if Known	
Application Number	TBD
Filing Date	HEREWITH
First Named Inventor	Li
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	2004 P 50201 US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	2	KING, A.C., *et al.*, "Surface Proximity Effect on End-of-Range Damage of Low Energy Ge^+ Implantation," Ultra Shallow Junctions 2003, Seventh International Workshop on: Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, April 27–May 1, 2003, pp. 447–450, Santa Cruz, CA, USA.	
	3	STRAUBE, U.N., *et al.*, "Adverse Effect of Ge^+ Implantation for Fabrication of SiGe PMOS," Electronics Letters, December 6, 2001, pp. 1549–1550, Vol. 37, No. 25.	
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	5	JIANG, H., *et al.*, "Electrical Properties of GeSi Surface- and Buried- Channel p-MOSFET's Fabricated by Ge Implantation," IEEE Transactions on Electron Devices, January, 1996, pp. 97–103, Vol. 43, No. 1, IEEE, New York, NY, USA.	
	6	JOHN, S., *et al.*, "Strained Si *n*-Channel Metal-Oxide-Semiconductor Transistor on Relaxed $Si_{1-x}Ge_x$ Formed by Ion Implantation of Ge," Applied Physics Letters, April 5, 1999, pp. 2076–2078, Vol. 74, No. 14, American Institute of Physics, College Park, MD, USA.	
	7	LIU, K.C., *et al.*, "A Deep Submicron $Si_{1-x}Ge_x$/Si Vertical PMOSFET Fabricated by Ge Ion Implantation," IEEE Electron Device Letters, January, 1998, pp. 13–15, Vol. 19, No. 1, IEEE, New York, NY, USA.	
	8	NGUYEN, N.V., *et al.*, "Characterization of the Interface Between Ge^+-Implanted Crystalline Silicon and its Thermally Grown Oxide by Spectroscopic Ellipsometry," Journal of Applied Physics, January 15, 1990, pp. 599–603, Vol. 67, No. 2, American Institute of Physics, College Park, MD, USA.	
	9	HÖCK, G., *et al.*, "High Hole Mobility in $Si_{0.17}Ge_{0.83}$ Channel Metal-Oxide-Semiconductor Field-Effect Transistors Grown by Plasma-Enhanced Chemical Vapor Deposition," Applied Physics Letters, June 26, 2000, pp. 3920–3922, Vol. 76, No. 26, American Institute of Physics, College Park, MD, USA.	
	10	SHANG, H., *et al.*, "High Mobility p-Channel Germanium MOSFETs with a Thin Ge Oxynitride Gate Dielectric," 2002, 0-7803-7463-X/02, IEEE, New York, NY, USA.	
	11	LEE, M.L., *et al.*, "Strained Ge Channel *p*-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown on $Si_{1-x}G_x$/Si Virtual Substrates," Applied Physics Letters, November 12, 2001, pp. 3344–3346, Vol. 79, No. 20, American Institute of Physics, College Park, MD, USA.	
	12	CHUI, C.O., *et al.*, "Germanium MOS Capacitors Incorporating Ultrathin High-κ Gate Dielectric," IEEE Electron Device Letters, August, 2002, pp. 473–475, Vol. 23, No. 8, IEEE, New York, NY, USA.	
	13	CHUI, C.O., *et al.*, "A Sub-400°C Germanium MOSFET Technology with High-κ Dielectric and Metal Gate," 2002, 0-7803-7463-X/02, IEEE, New York, NY, USA.	
	14	ZOLLNER, S., *et al.*, "Optical Constants and Ellipsometric Thickness Determination of Strained $Si_{1-x}Ge_x$:C Layers on Si (100) and Related Heterostructures," Journal of Applied Physics, October 1, 2000, pp. 4102–4108, Vol. 88, No. 7, American Institute of Physics, College Park, MD, USA.	
	15	LEGOUES, F.K., *et al.*, "Oxidation Studies of SiGe," Journal of Applied Physics, February 15, 1989, pp. 1724–1728, Vol. 65, No. 4, American Institute of Physics, College Park, MD, USA.	
	16	PLUMMER, et al., Silicon VLSE Technology, Fundamentals, Practice and Modeling, 2000, p. 453, Prentice Hall, Upper Saddle River, NJ.	
	17	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2002 Update, pp. 45–62, http://member.itrs.net/.	
	18	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23–25, http://member.itrs.net/.	

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